A fully digital power supply noise thermometer

A FULLY DIGITAL POWER SUPPLY NOISE *THERMOMETER*

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ABSTRACT—Power Supply Noise (PSN) is one of the main concerns in scaled technology circuits, both if performance reliability must be assured and if power supply is to be dynamically reduced for dissipation regulation. In this paper we propose a new system for digitally sensing Power Supply and Ground levels that can be both transferred to the output for verification purposes and used by a control block within the circuit under test (CUT) for the activation of power aware policies. The sensor system shows very low overhead in terms of power and area, and works at the nominal CUT frequency. It allows to change on-site the Power Supply and Ground ranges to be sensed and, after a fine tuning, can be arranged for a process variation aware measures. This sensor is fully digital and standard cell based and can be used for every type of architecture on a systematic basis for PSN measure as scan chains are for fault verification. It thus represents a change of paradigm in the way in which PSN measure systems are thought nowadays.

I. INTRODUCTION

Power Supply Noise (PSN) is a well known problem in scaled technologies. Its understanding has deeply changed in the last years, together with the countermeasures for keeping it limited. For example, in [1] a point of view is given on the problem nature and on the possible solutions, while in [2] a more recent analysis can be found about the strict relation between on-die and package PSN and about the possible methodologies to mitigate it. To further rapidly overview the problem the work in [3] should be examined for understanding the difference between static and dynamic PSN.

The classic solutions techniques were “a priori”: noise amount was estimated during circuit design and thus design methodologies were suggested to reduce it, as, for example, in [1] and in [4]. Recently, the problem is more “actively” observed and tackled with two main goals: to know exactly the PSN amount and to exploit dynamic Power Supply (PS) decreasing for power dissipation reduction. In any case accurate on-site PS measurement systems are needed and among all the proposed solutions an interesting example is in [5] where an advanced analog on-chip sampler is used to measure PS.

As on-chip ancillary analog circuits are critical and justified for high-performance and top level designs only, digital systems have been recently explored as a viable solution to assure still reliable results in digital circuits under test. In [6] an ad-hoc digital circuit has been proposed which allows to achieve a general information on the on chip general error probability due to PSN. Thought an interesting solution, it requires a careful design and gives a general information, which is difficult to be used, especially in power-aware architectures. In [7] a fully digital standard-cell based circuit for capturing PS noise waveforms is proposed. This is a powerful solution for verification purposes, but it cannot be used in power-aware architectures; furthermore, as it is based on a ring oscillator, it cannot distinguish between power and ground voltage variations. In [8] a digital system is integrated within the computational flow of a processor. It can be aware, within given ranges, of PSN induced errors due to an excessive reduction of PS forced for power dissipation reduction purposes, and can partially recover them acting at the data flow level. This solution is highly interesting, though it requires a careful design of the sense block and of the recovering system which is suitable for a pipeline based processor, and not for a general architecture.

In this paper we propose a circuit able to give a digital information proportional to Vdd or to Gnd (or both), which can be used in any type of architecture and can be repeated in many points of the circuit on a systematic basis for PSN measure, and thus can be thought as a PSN scan chain. It is suitable for both verification purposes or for power-aware techniques. It inherits some features from [6], [7] and [8], but it is strongly new for its simplicity, usability in a scan-chain-like philosophy and its flexibility of application. Furthermore it is fully digital and standard cell based, the measure range can be dynamically adapted, and it can be configured to be process variation aware. The paper presents in section II the basic idea, while in section III the whole structure and main results are briefly discussed. In section IV conclusions are drawn.

II. NOISE SENSOR

The proposed circuit is based on the key element in figure 1(left) based on an inverter, a flip-flop (FF) and a load *C*. The inverter (INV) is connected to the PS *VDD-n* and Ground *GND-n* to be measured; its output node *delay-sense (DS)*, loaded by C if necessary (see next section), is the FF input node, which is powered by “nominal” power and ground signals. Both INV and FF are standard cells; the load C can be realized by a transistor conveniently connected. The INV input P and the FF clock CP must have a known delay relation. Let’s suppose that at “nominal” supply and ground conditions P is such that DS respects the FF set-up time: the FF will correctly sample P. On the contrary, if, with an identical P and CP relation, for example, *VDD-n* is reduced, DS will be delayed so that set-up time may be violated, and

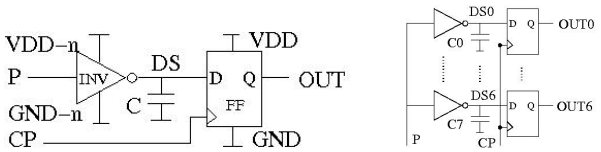

Fig. 1. Left: Noise sensor; P: input pulse, CP: sensor clock, DS: delay-sense, OUT: sensor output, VDD-n: noisy supply, GND-n: noisy reference signal. Right: Sensor array: identical control signals and sizes; increasing capacitance.

so that the FF may fail the evaluation. An ELDO post-layout simulation of this circuit based on 90nm standard cells is in figure 2. Signal DS linearly increases as a linear decrease of *VDD-n* is forced (for example [9] shows that within given ranges the relation is linear). OUT delay increases in a not linear way as the FF is in its metastability state and, in the last case (4) a fail occurs.

The system which exploits this sensor is organized so that a sequence is repeated of SENSE phase, that is the FF evaluation, and PREPARE phase, necessary so that each measure is repeated always in the same conditions, and that an error can be caused only by the current PS value. Figure 3 shows an ELDO post-layout simulation of two sequences: the first for a nominal $VDD = 1V$ and the second for a $VDD = 0.95V$, both organized in PREPARE and SENSE phases. In the PREPARE phase, DS, and thus OUT, are forced low (P=1); in the SENSE phase DS is forced high (P=0) so that there is a delay dependence from *VDD-n*; if the *GND-n* is to be sensed, then the PREPARE and and SENSE conditions are opposite. As clear form the simulation, the first measure gives a "1" while the second gives a "0" as the set-up time is violated.

III. THERMOMETER ARCHITECTURE

A. Single and Multiple bit sensor characterisation

The *VDD-n* (or *GND-n*) value which causes DS to violate the FF set-up time depends on the relation between CP and P and on INV and FF transistor sizes. As these are library values, such sizes are known and fixed. For varying the sensibility to the *VDD-n* failure threshold, we propose to change the load C at DS: the greater is the load, the slower is DS, the easier is the sense error occurrence, and thus the higher is the *VDD-n* causing it. In figure 4 we show the sensor characteristic (post-layout ELDO simulation) as the *VDD-n* value below which the FF fails as a function of the capacitance C. For example,

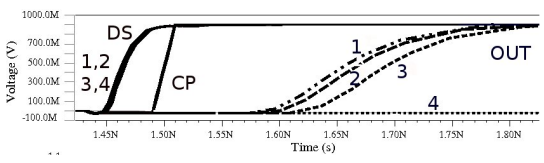

Fig. 2. Noise sensor detail: DS signal has increasing propagation delay with respect to input pulse P (cases 1-4 having linear distance); OUT sample is correct in cases 1,2,3, wrong in case 4.

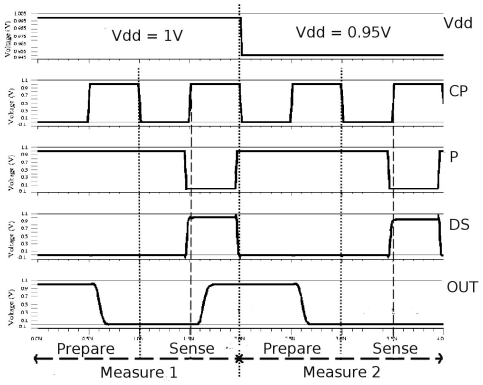

Fig. 3. Sequence of two measures organized in two phases: PREPARE and SENSE. First measure: nominal VDD and DS, respected set-up time, correct OUT sample. Second measure: noisy VDD, delayed DS signal, violated set-up time, wrong OUT sample.

if C=2pF (added to the intrinsic DS node capacitance), the *VDD-n* value below which the FF fails is 0.9360V. Note that, the characteristic has a linear behavior within the *VDD-n* range of interest (0.9V - 1.1V in this example). This behavior thus suggests the idea to organize a multi-bit sensor as in figure 1(right) (in this example 7 bits are chosen), in which INV-i and FF-i are identical, while, the capacitor at DS-i increases linearly so that each FF has a different threshold. This structure is thus a noise "thermometer" and in principle is similar to a flash A/D converter: the digital output vector is proportional to the *VDD-n* value.

The output OUT-i can assume all '1' values (none error occurred, *VDD-n* is above the maximum measurable value), all '0' values (all errors, *VDD-n* is below the minimum measurable value), or an intermediate configuration. In figure 5 three examples of the array characteristic are reported for three delay relations between P and CP (see later for the delay code meaning): for each delay case the *VDD-n* dynamic is shown and the correspondent multi-bit sensor output vector is in the x-axis. For example, in the delay code 011 case, the threshold range goes from 0.827V (all errors) to 1.053V (no errors); for the intermediate threshold cases the sensor output will have, for example, code 0011111 if *VDD-n* is lower than

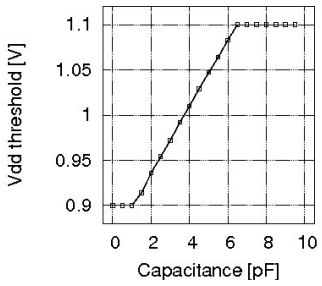

Fig. 4. Sensor sensitivity characterization: Vdd threshold for a correct FF sampling with varying capacitances at DS.

1.021V and greater than 0.992V.
In case the delay code is 010, the dynamic ranges from 0.951V to 1.237V (also overvoltages can be measured then if interesting). This is due to a lower delay between P and CP, thus an higher set-up error possibility: as a consequence, only *VDD-n* values higher than the previous delay case allow the FF to correctly sample DS. This shows that a variation of P and CP, conveniently trimmed, allows to dynamically change the multibit sensor dynamic, or to compensate the different sensor behavior in presence of process variations (of course having as an input an information on the process corner and having a careful characterization of the sensor in such condition). In fact, for example, in slow conditions, the INV is slower and thus the *VDD-n* threshold value is lower: the CP-P delay necessary to achieve the same characteristic should be lower. Similar characterics have been generated for other delay codes and for the *GND-n* measure, but not reported for sake of brevity.

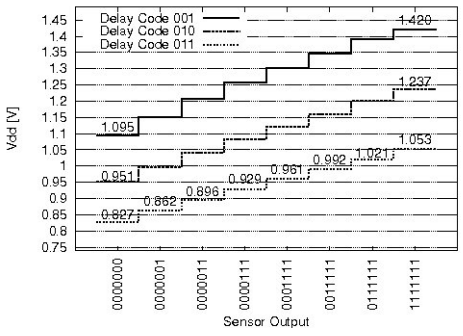

Fig. 5. Multibit sensor characteristic for three CP-P delay relations.

B. Sensor system

The multibit sensor is managed by a digital control system which receives the measured data, organizes the measure phase and communicates with the external blocks (e.g. off-chip blocks or on-chip control block of the CUT). The system block diagram is in figure 6. An INV array senses *VDD-n*, and will be mentioned herein as HIGH-SENSE (HS); another INV array senses *GND-n*, called LOW-SENSE (LS). The separation allows to have different measures for *VDD-n* and *GND-n* and is also convenient to avoid measure interferences. In fact, HS-INV have "nominal" Ground, and, viceversa, LS-INV have "nominal" PS. The INV arrays are connected to FF arrays, whose output are encoded by the ENC block in a noise word OUTE. OUTE is the input of the control (CNTR) which gives to the output the measured data and receives configurations. Furthermore it manages a counter and a pulse-generator (PG) which allows to generate the P and CP signal to the sensor with the correct delay relation. The FFs and all the other digital blocks have "nominal" PS and Ground; this means that they do not need to be carefully controlled as for an analog circuit; they simply

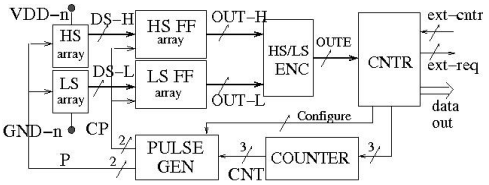

Fig. 6. Architecture block diagram: sensor and control system.

should have a dedicated power supply pin, so that the control system can work reasonably unaffected by the CUT power supply system (clearly the FFs could be slightly affected by a PS variation causing a measure error that should be characterized). Note also that the sensor arrays (INVs plus FFs) can be multiplied, so that measures in many points of the CUT are possible. The critical path of the whole control system at 90nm is 1.22ns, thus it can work with most of the typical CUTs system clock.

An interesting block is the PG, schematically reported in figure 7. Signals CP_to_PG and P_to_PG are forced by CNTR or by the COUNTER (details are not reported for sake of brevity): at the PG output, P and CP are delayed thanks to delay element arrays (standard cell INV with opportunely chosen sizes). The delay is chosen by the control setting the delay_HS (*delay_LS*) signal. As the MUX inserts a further delay, the same MUX is also used for the P signal, so that P and CP are skewed of the same value. P and CP require also an accurate routing as they were a differential pair (a delay introduced by routing on both does not influence the measure but only the moment in which the measure is executed, while the skew between them must be accurately checked). In our example the delays an their correspondent Delay Code are:

Delay Code	000	001	010	011	100	101	110	111
CP delay [ps]	26	40	50	65	77	92	100	107

Another interesting block is CNTR, which is mainly based on a FSM which flow transition diagram is in figure 8. After the RESET the FSM remains in the IDLE state until the noise measure is enabled by external signals. From the READY state, depending on extern control bits, the system is initialized and then the normal PREPARE (in the states S_PRP0 for the negative CP edge and S_PRP for the positive CP edge with P=1) SENSE (in the state READY in which the negative CP edge again is generated and then the very sense phase with P=0) sequence is generated. The control can receive from the external circuits the Delay Code or can define and set them internally according to a policy not reported for sake

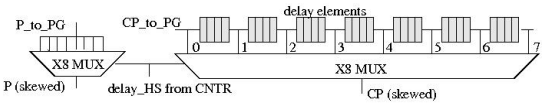

Fig. 7. Pulse generator block diagram.

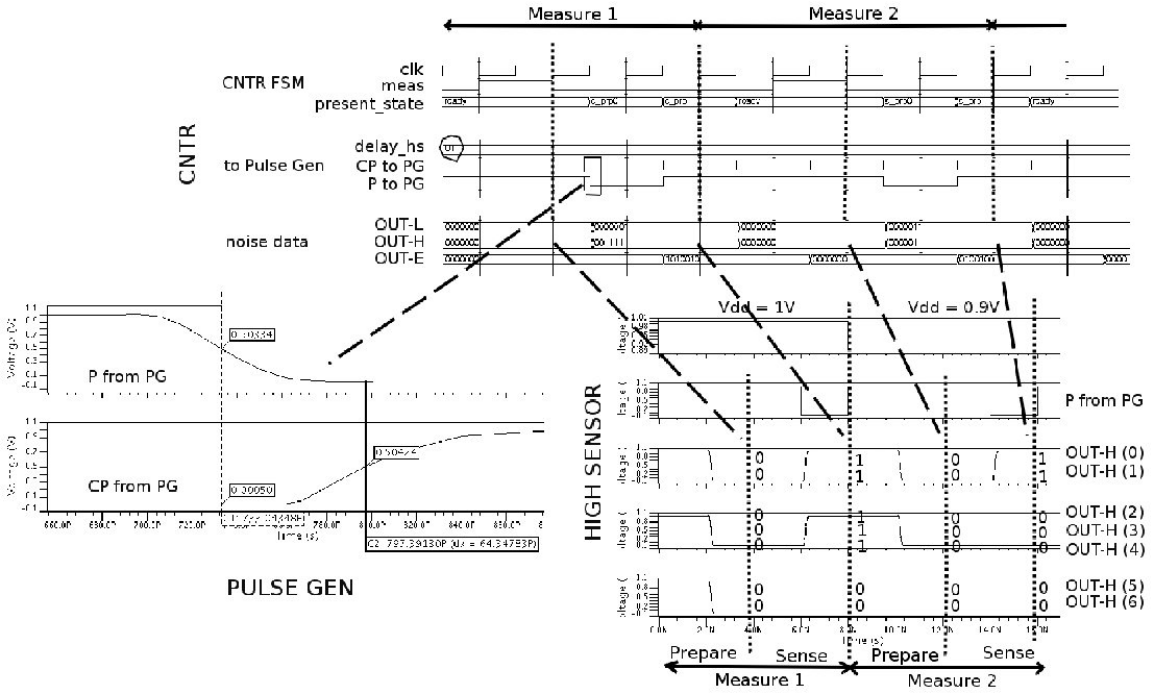

Fig. 9. Example of the system behavior for a sequence of two measures.

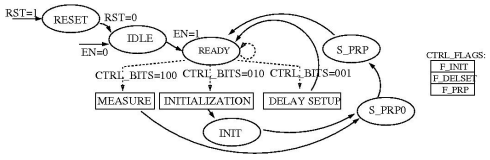

Fig. 8. Simplified flow diagram of the control block.

of brevity. Furthermore, measures should be iterated so that noise values can be captured in different moments of the CUT transient behavior.

Finally, in figure 9 an example of how the system works for two measures (*VDD-n*=1V and *VDD-n*=0.9V) is reported in which a few CNTR, PG end HS signals are shown. The Delay Code introduced is 011 that is a delay of 65ps: this is evidenced in the left detail where the P and CP from the CNTR are transformed in the delayed signals from the PG. As underlined during the PREPARE phase the sensor output is '0000000'; while after the SENSE the values '0011111' and '0000011' are found respectively for the first and the second measure. According to the characteristic curve in figure 5, 0011111 corresponds to a *VDD-n* in the range 0.992V-1.021V, while 0000011 to the range 0.896V-0.929V. The measures are thus reflecting the two 'input' noise values.

IV. CONCLUSIONS

We have proposed a sensor system for measuring power supply and ground voltages of a CUT. The system is fully digital and standard cell based and does require only slightly accurate design solution to assure appropriate behavior. The sensor dynamic can be easily dynamically changed. By means of the same strategy it can be adapted so that measures are process variation insensitive. The array sensors can be placed in many points of the DUT, whilst only a control system is required. This sensor system can be thought for PSN as scan chains are for data faults, and can be used for verification purposes or for setting-up power aware strategies within the CUT, which can be a general digital architecture.

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